LME49830 Mono High Fidelity 200 Volt MOSFET Power Amplifier Input Stage with Mute

Check for Samples: LME49830

FEATURES

- **High Output Current and Voltage for Use With MOSFET Output Stages**
- **Very High Voltage Range: ±20V to ±100V**
- **Scalable Output Power**
- **Minimum External Components**
- **External Compensation**
- **Thermal Shutdown of Input Stage**
- **Mute Control**

APPLICATIONS

- **AV Receivers**
- **Audiophile Power Amps**
- **Pro Audio**
- **High Voltage Industrial Applications**

KEY SPECIFICATIONS

- **Wide Operating Voltage Range: ±20V to ±100V**
- **Output Voltage Noise**
  - **(BW = 30kHz): 44µV (Typ)**
- **PSRR (DC): 105dB (Typ)**
- **Slew Rate: 39V/µs (Typ)**
- **THD+N (f = 1kHz): 0.0006% (Typ)**

DESCRIPTION

The LME49830 is a high fidelity audio power amplifier input stage designed for demanding consumer and pro-audio applications. Amplifier output power may be scaled by changing the supply voltage and number of output devices. The LME49830 is capable of driving an output stage in excess of 300 W single-ended into an 8Ω load in the presence of 10% high line headroom and 20% supply regulation.

The LME49830 includes internal thermal shut down circuitry that activates when the LME49830 die temperature exceeds 150°C. The LME49830 has a mute function that mutes the input drive signal and forces the amplifier output to a quiescent state.

The LME49830 has high drive current, 56mA typical, and high output voltage swing for maximum flexibility in output stage choice. With a bias voltage range up to 16V the LME49830 can be used to drive MOSFET output stages using a wide selection of MOSFETs.

The LME49830 has a wide operating supply range of ±20V to ±100V, which allows lower cost, unregulated power supplies to be used.

Typical Application

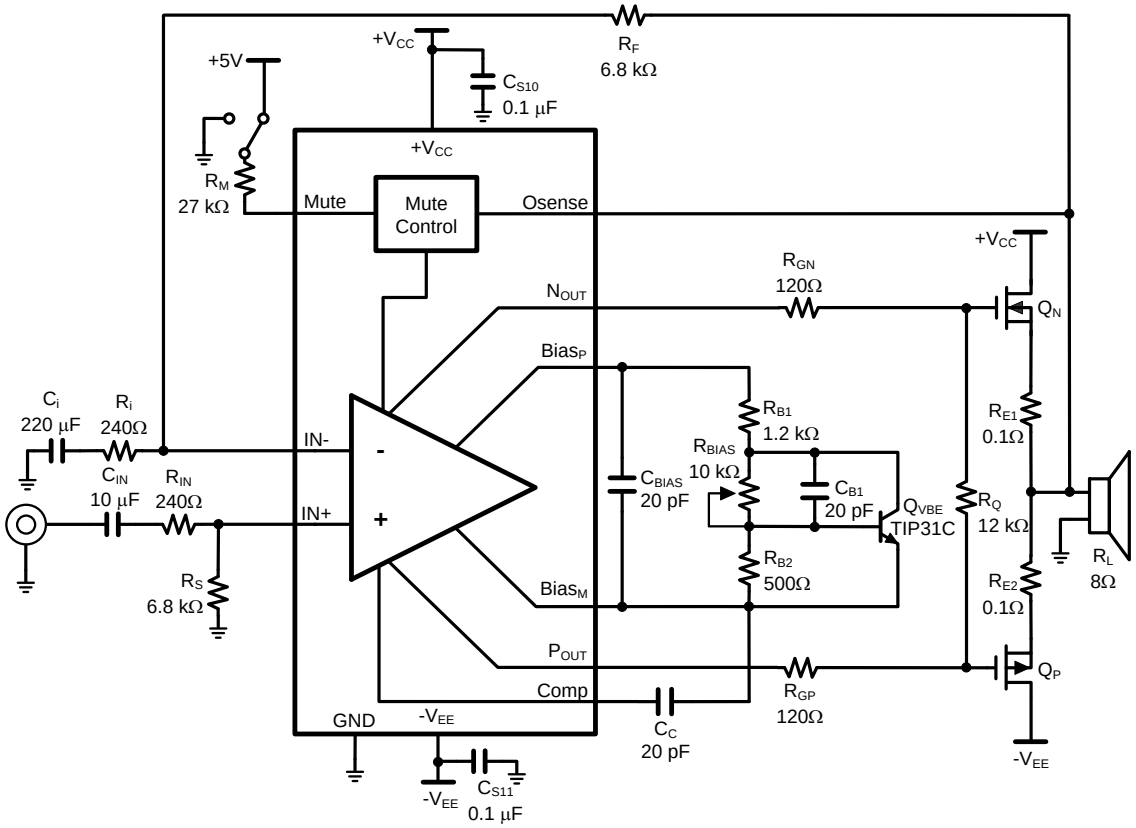

Figure 1. Typical Audio Amplifier Application Circuit

CONNECTION DIAGRAM

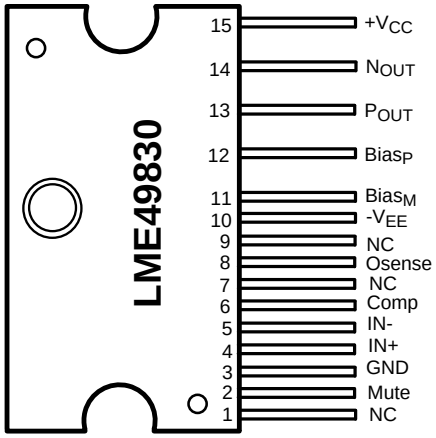

Figure 2. Plastic Package(1) (Top View)

(1) The NDN0015A is a non-isolated package. The package's metal back and any heat sink to which it is mounted are connected to the V_{EE} potential when using only thermal compound. If a mica washer is used in addition to thermal compound, θ_{CS} (case to sink) is increased, but the heat sink will be electrically isolated from V_{EE}.

PIN DESCRIPTIONS

Pin	Pin Name	Description
1	NC	No Connection, Pin electrically isolated
2	Mute	Mute Control
3	GND	Device Ground
4	IN+	Non-inverting input
5	IN-	Inverting input
6	Comp	External Compensation Connection
7	NC	No Connection, Pin electrically isolated
8	Osense	Output Sense
9	NC	No Connection, Pin electrically isolated
10	$-V_{EE}$	Negative Power Supply
11	$Bias_M$	Negative External Bias Control
12	$Bias_P$	Positive External Bias Control
13	P_{OUT}	P-channel MOSFET Output
14	N_{OUT}	N-channel MOSFET Output
15	$+V_{CC}$	Positive Power Supply

BLOCK DIAGRAM

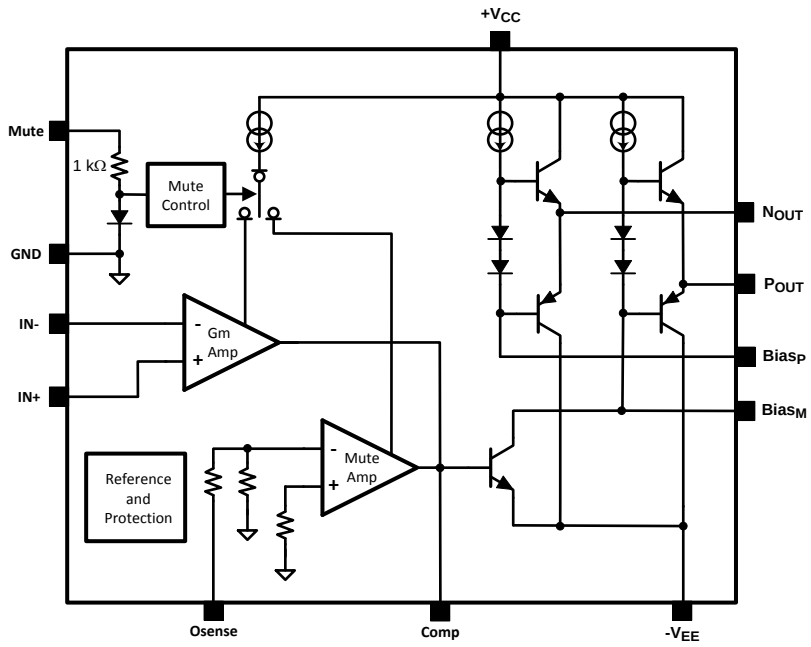

Figure 3. LME49830 Simplified Block Diagram

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)(3)

Supply Voltage $\|V^+\| + \|V^-\|$		200V
Differential Input Voltage		+/-6V
Common Mode Input Range		0.4 V_{EE} to 0.4 V_{CC}
Power Dissipation(4)		5.4W
ESD Rating(5)		2.0kV
ESD Rating(6)		200V
Junction Temperature (T_{JMAX})		150°C
Soldering Information	NDN Package (10 seconds)	260°C
Storage Temperature		-40°C to +150°C
Thermal Resistance	θ_{JA}	73°C/W
	θ_{JC}	4°C/W

(1) The Electrical Characteristics tables list ensure specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LME49830, T_{JMAX} = 150°C and the typical θ_{JC} is 4°C/W.
(5) Human body model, applicable std. JESD22-A114C.
(6) Machine model, applicable std. JESD22-A115-A.

OPERATING RATINGS(1)(2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le +85°C$
Supply Voltage		$\pm 20V \le V_{SUPPLY} \le \pm 100V$

(1) The Electrical Characteristics tables list ensure specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
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ELECTRICAL CHARACTERISTICS V_{CC} = +100V, V_{EE} = –100V[1][2]

The following specifications apply for I_{MUTE} = 150µA unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LME49830		Units (Limits)
			Typical[3]	Limit[4]	
I_{CC}	Total Positive Quiescent Power Supply Current	V_{IN} = 0V, V_O = 0V, I_O = 0A	19	24	mA (max)
I_{EE}	Total Negative Quiescent Power Supply Current	V_{IN} = 0V, V_O = 0V, I_O = 0A	–21		mA
THD+N	Total Harmonic Distortion + Noise	No load, f = 1kHz, A_V = 30dB V_{OUT} = 30V_{RMS}, 30kHz BW	0.0006		%
V_{BIAS}	Bias Voltage		16	15	V (min)
$A_{V(CL)}$	Closed Loop Voltage Gain			26	dB (min)
$A_{V(OL)}$	Open Loop Gain	f = DC V_{IN} = 1mV_{RMS}, f = 1kHz, C_C = 10pF	112 88	82	dB (min)
V_{OM}	Output Voltage Swing	THD = 0.05%, f = 20Hz to 20kHz	68		V_{RMS}
V_{NOISE}	Output Noise	R_S = 10kΩ, A_V = 30dB, 30kHz BW A-weighted	44 28	 205	µV µV (max)
I_{OUT}	Maximum Output Current	Current from Output pins	56	47	mA (min)
I_{MUTE}	Current into Mute Pin	To put part in “play” mode		130	µA (min)
SR	Slew Rate	V_{IN} = 1.2V_{P-P}, A_V = 30dB, f = 10kHz square wave, C_{LOAD} = 2,000pF	39		V/µs
V_{OS}	Input Offset Voltage	V_{CM} = 0V, I_O = 0mA, I_{MUTE} = 150µA	±0.9	±3	mV (max)
		V_{CM} = 0V, I_O = 0mA, I_{MUTE} = 0µA	±0.4	±4.2	mV (max)
I_B	Input Bias Current	V_{CM} = 0V, I_O = 0mA	95	250	nA (max)
$PSRR_{AC}$	Power Supply Rejection Ratio (AC)	R_S = 1kΩ, f = 100Hz,V_{RIPPLE} = 1V_{RMS}, Input Referred, A_V = 30dB	104		dB
$PSRR_{DC}$	Power Supply Rejection Ratio (DC)	R_S = 1kΩ, Input Referred, A_V = 30dB	105	94	dB (min)
I_{AB}	Bias Control Current	Shorted output, shorted bias control	2	1.6 2.7	mA (min) mA (max)

(1) The Electrical Characteristics tables list ensure specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.

(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.

(3) Typical values represent most likely parametric norms at T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization.

(4) Data sheet min and max specification limits are specified by test or statistical analysis.

Test Circuit Diagram

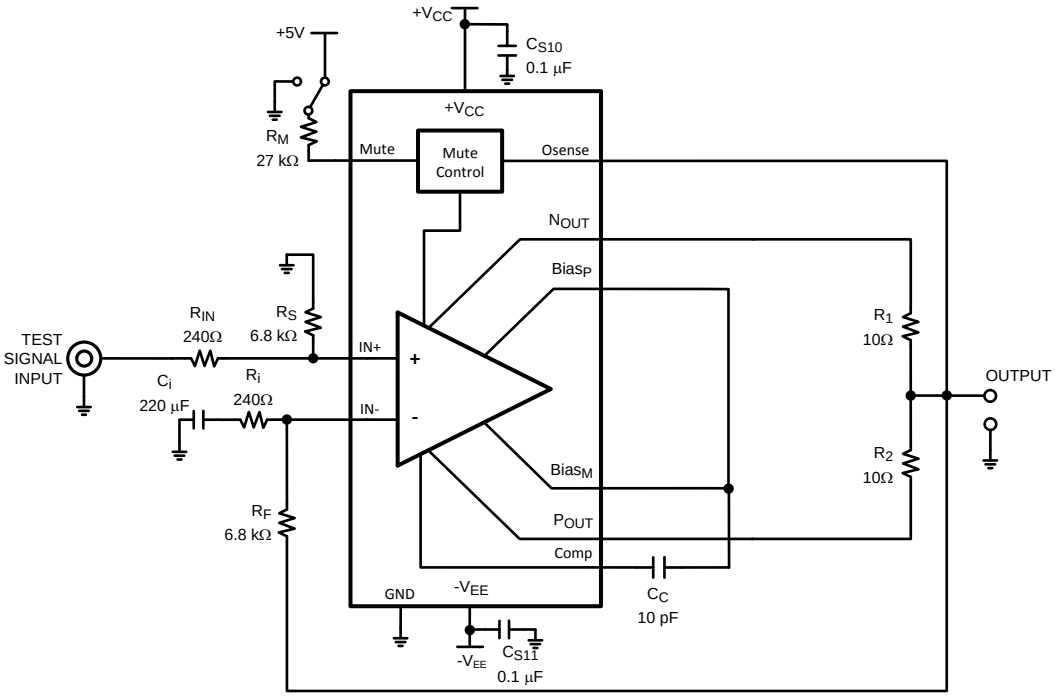


Figure 4. LME49830 Test Circuit Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

THD+N vs Frequency
$+V_{CC} = -V_{EE} = 20V$, $V_O = 5V$

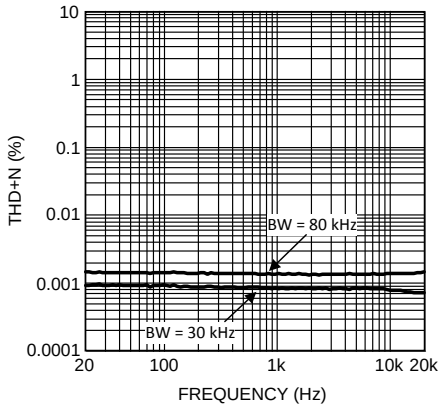


Figure 5.

THD+N vs Frequency
$+V_{CC} = -V_{EE} = 20V$, $V_O = 10V$

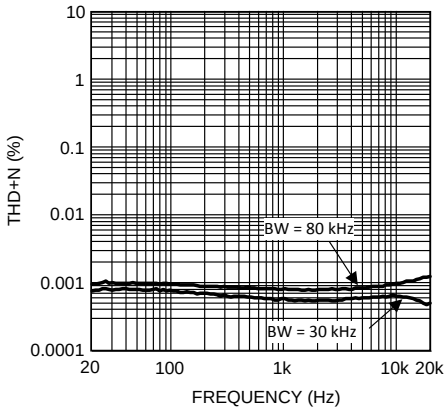


Figure 6.

THD+N vs Frequency
$+V_{CC} = -V_{EE} = 50V$, $V_O = 14V$

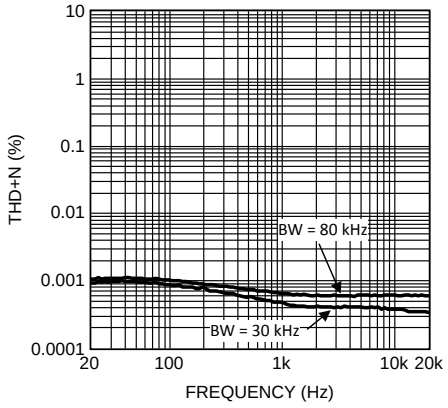


Figure 7.

THD+N vs Frequency
$+V_{CC} = -V_{EE} = 50V$, $V_O = 20V$

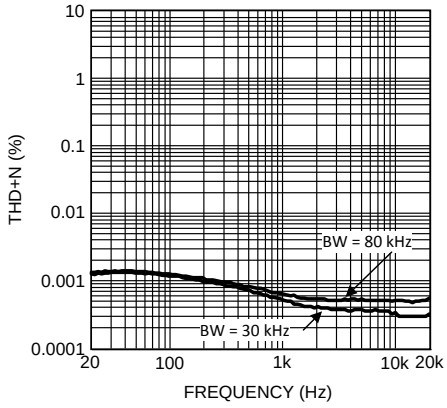


Figure 8.

THD+N vs Frequency
$+V_{CC} = -V_{EE} = 100V$, $V_O = 14V$

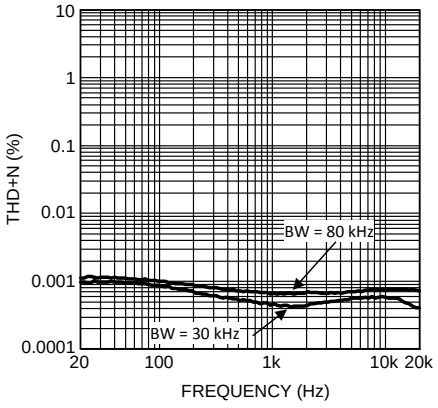


Figure 9.

THD+N vs Frequency
$+V_{CC} = -V_{EE} = 100V$, $V_O = 30V$

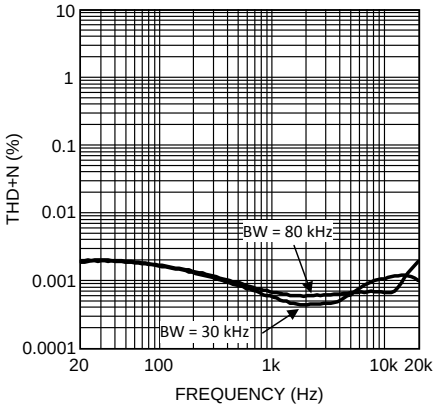


Figure 10.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

THD+N vs Output Voltage
$+V_{CC}$ = $-V_{EE}$ = 50V, f = 20Hz

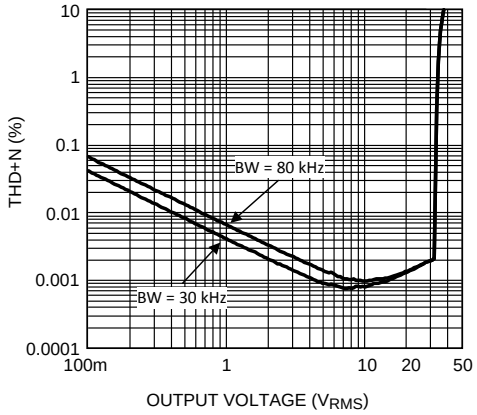


Figure 11.

THD+N vs Output Voltage
$+V_{CC}$ = $-V_{EE}$ = 100V, f = 20Hz

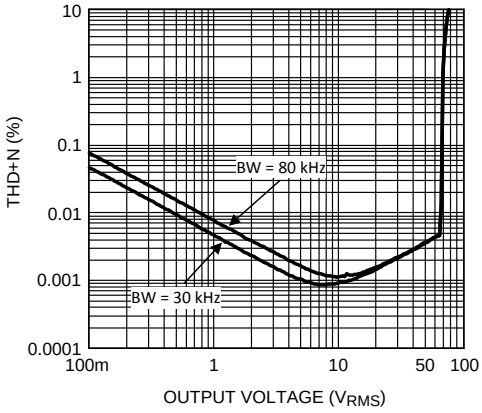


Figure 12.

THD+N vs Output Voltage
$+V_{CC}$ = $-V_{EE}$ = 50V, f = 1kHz

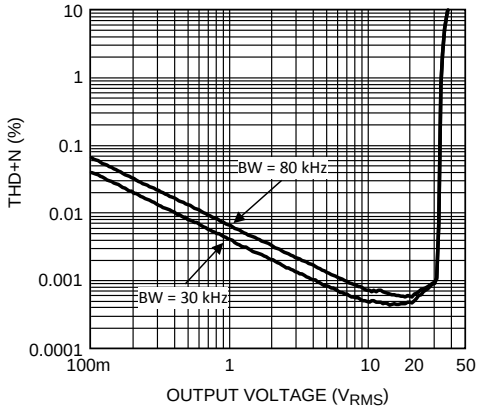


Figure 13.

THD+N vs Output Voltage
$+V_{CC}$ = $-V_{EE}$ = 100V, f = 1kHz

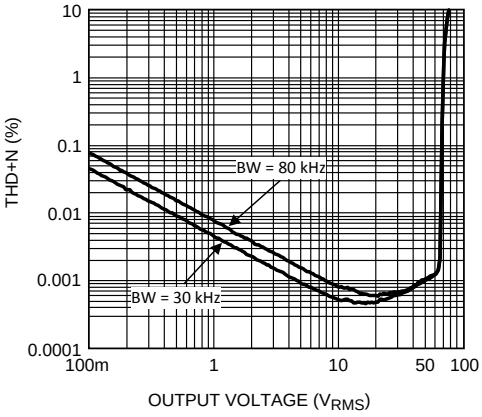


Figure 14.

THD+N vs Output Voltage
$+V_{CC}$ = $-V_{EE}$ = 50V, f = 20kHz

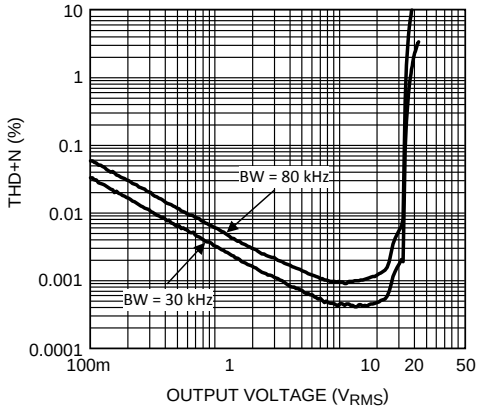


Figure 15.

THD+N vs Output Voltage
$+V_{CC}$ = $-V_{EE}$ = 100V, f = 20kHz

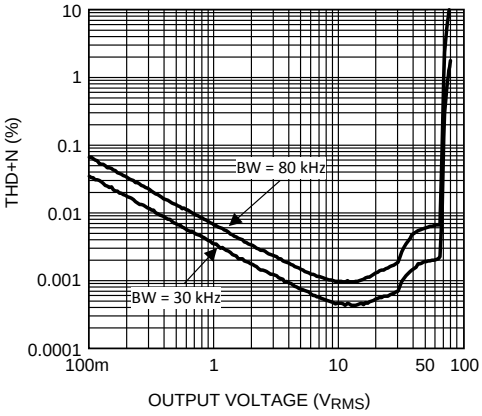


Figure 16.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

THD+N vs Output Voltage
$+V_{CC} = -V_{EE}$ = 20V, f = 20Hz

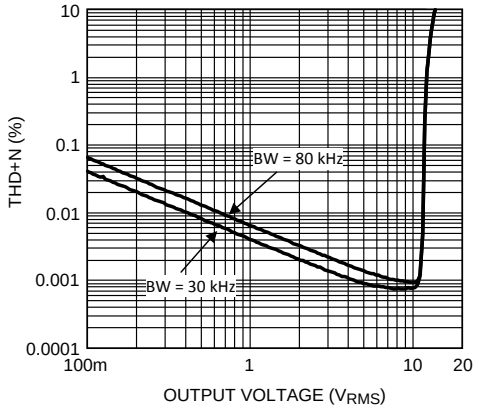


Figure 17.

THD+N vs Output Voltage
$+V_{CC} = -V_{EE}$ = 20V, f = 1kHz

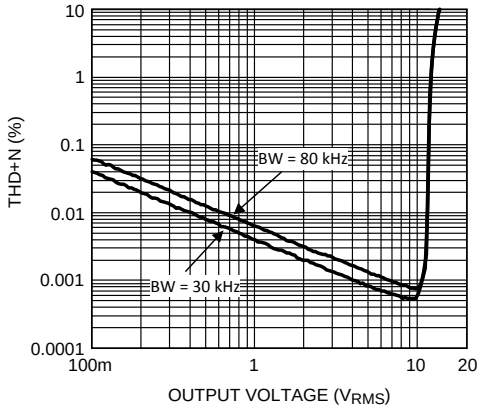


Figure 18.

THD+N vs Output Voltage
$+V_{CC} = -V_{EE}$ = 20V, f = 20kHz

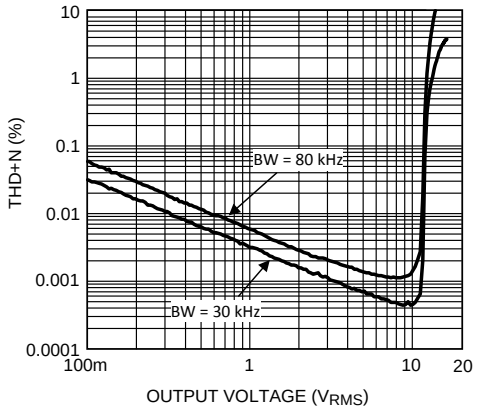


Figure 19.

Closed Loop Frequency Response
$+V_{CC} = -V_{EE}$ = 50V, V_{IN} = 1V_{RMS}

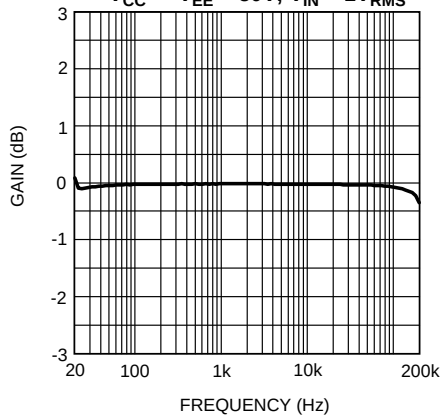


Figure 20.

Closed Loop Frequency Response
$+V_{CC} = -V_{EE}$ = 100V, V_{IN} = 1V_{RMS}

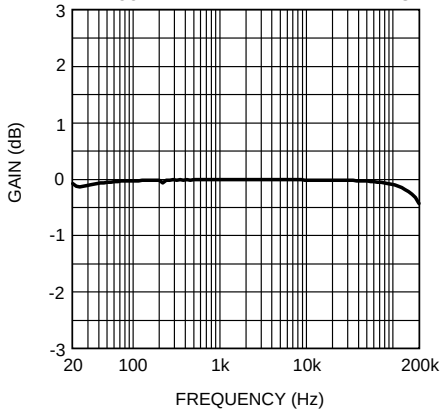


Figure 21.

PSRR vs Frequency
$+V_{CC} = -V_{EE}$ = 100V, No Filters, Input Referred
V_{RIPPLE} = 200mV_{RMS} on V_{CC} pin

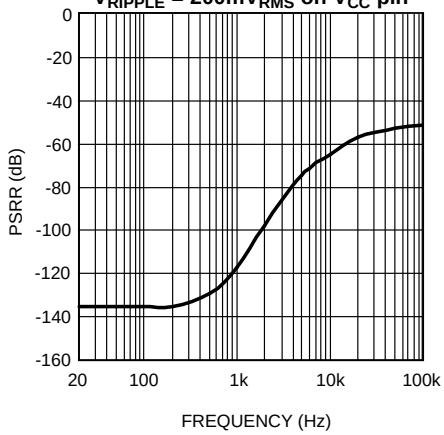


Figure 22.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

PSRR vs Frequency
$+V_{CC}$ = $-V_{EE}$ = 100V, No Filters, Input Referred
V_{RIPPLE} = 200mV_{RMS} on V_{EE} pin

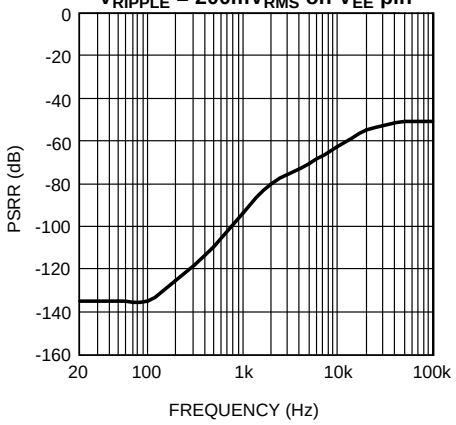


Figure 23.

Mute Attenuation vs I_{MUTE}
$+V_{CC}$ = $-V_{EE}$ = 100V

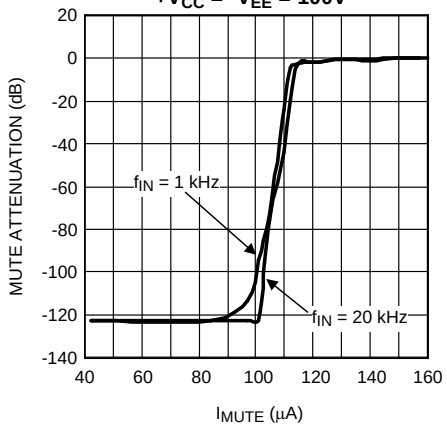


Figure 24.

Output Voltage vs Supply Voltage

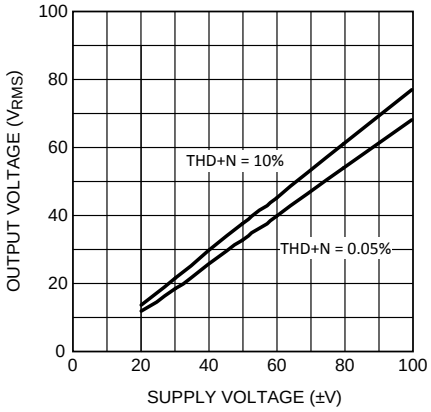


Figure 25.

Slew Rate vs Compensation Capacitor
$+V_{CC}$ = $-V_{EE}$ = 100V, V_{IN} = 1.2V_P, No Load

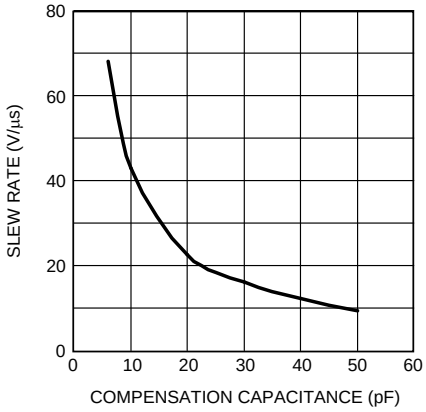


Figure 26.

Supply Current vs Supply Voltage

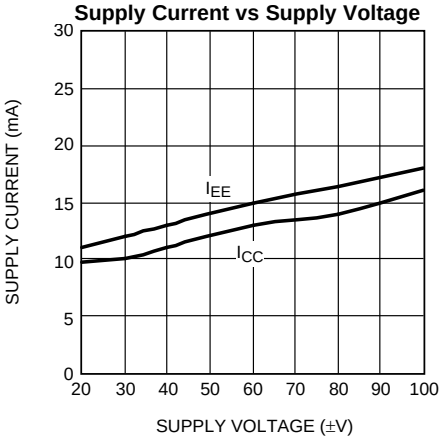


Figure 27.

Input Offset Voltage vs Supply Voltage

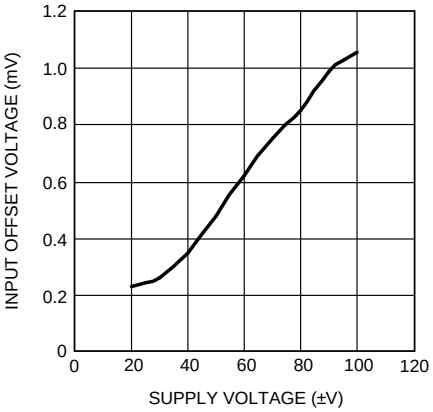


Figure 28.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Open Loop Gain and Phase Margin
$+V_{CC} = -V_{EE} = 100V$

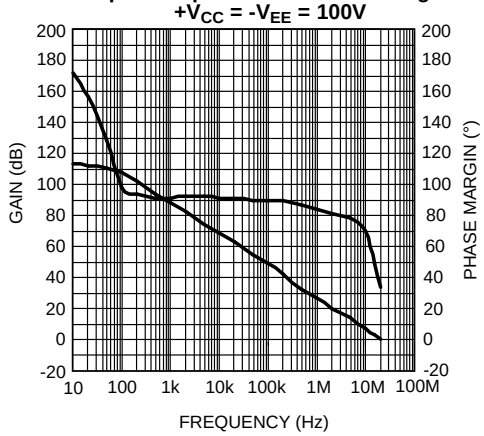


Figure 29.

CMRR vs Frequency
$+V_{CC} = -V_{EE} = 100V$

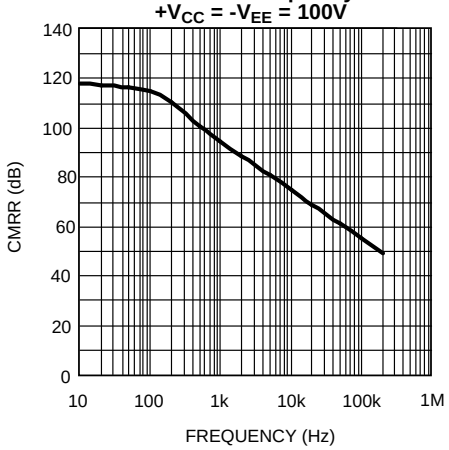


Figure 30.

Noise Floor
$+V_{CC} = -V_{EE} = 50V$, $V_{IN} = 0V$

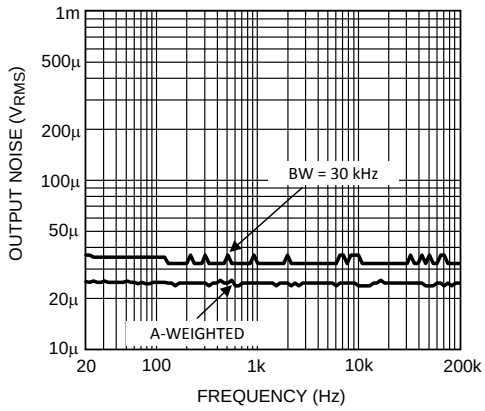


Figure 31.

Noise Floor
$+V_{CC} = -V_{EE} = 100V$, $V_{IN} = 0V$

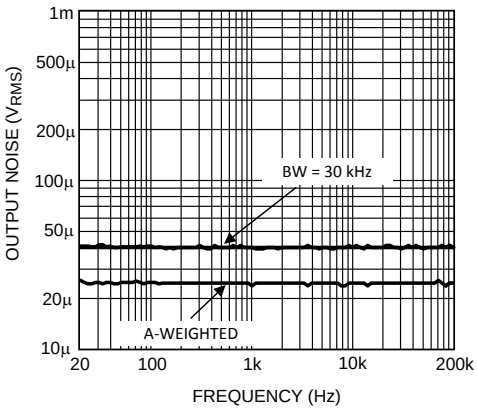


Figure 32.

APPLICATION INFORMATION

MUTE FUNCTION

The mute function of the LME49830 is controlled by the amount of current that flows into the MUTE pin. If there is less than 100µA of current flowing into the MUTE pin, the part will be in mute mode. This can be achieved by shorting the MUTE pin to ground. It is recommended to connect a capacitor C_M (its value not less than 47µF) between the MUTE pin and ground for reducing voltage fluctuation when switching between 'play' and 'mute' mode. If there is between 130µA and 2mA of current flowing into the MUTE pin, the part will be in 'play' mode. This can be done by connecting a power supply, V_{MUTE}, to the MUTE pin through a resister, R_M. The current into the MUTE pin can be determined by the equation $I_{MUTE} = (V_{MUTE} - V_{BE}) / (1k\Omega + R_M)$ (A), where $V_{BE} \cong 0.7V$. For example, if a 5V power supply is connected through a 27kΩ resistor to the MUTE pin, then the mute current will be 154µA, at the center of the specified range. It is also possible to use V_{CC} as the power supply for the MUTE pin, though R_M will have to be recalculated accordingly. It is not recommended to flow more than 2mA of current into the MUTE pin because damage to the LME49830 may occur.

THERMAL PROTECTION

When the temperature on the die exceeds 150°C, the LME49830 shuts down. It starts operating again when the die temperature drops to about 145°C. When in thermal shutdown, the current supply internal to the LME49830 will be cut-off. There will be no signal generated to the output while in thermal shutdown. After the die temperature decreases, the LME49830 will power up again and resume normal operation. If the fault conditions continue, thermal protection will be activated and repeat the cycle preventing the LME49830 from over heating.

Since the die temperature is directly dependent upon the heat sink used, the heat sink should be chosen so that thermal shutdown is not activated during normal operation. Using the best heat sink possible within the cost and space constraints of the system will improve the long-term reliability of any power semiconductor device, as discussed in the DETERMINING THE CORRECT HEAT SINK section. It is recommended to use a separate heat sink from the output stage heat sink for the LME49830. A heat sink may not be needed if the supply voltages are low.

POWER DISSIPATION AND HEAT SINKING

When in "play" mode, the LME49830 draws a constant amount of current, regardless of the input signal amplitude. Consequently, the power dissipation is constant for a given supply voltage and can be computed with the equation $P_{DMAX} = I_{CC} \times (V_{CC} - V_{EE})$ (W). For a quick calculation of P_{DMAX}, approximate the current to be 20mA and multiply it by the total supply voltage (the current varies slightly from this value over the operating range).

DETERMINING THE CORRECT HEAT SINK

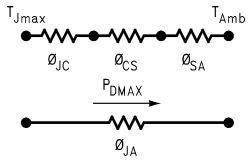
The choice of a heat sink for any power IC is made entirely to keep the die temperature at a level such that the thermal protection circuitry is not activated under normal circumstances.

The thermal resistance from the die to the outside air, θ_{JA} (junction to ambient), is a combination of three thermal resistances, θ_{JC} (junction to case), θ_{CS} (case to sink), and θ_{SA} (sink to ambient). The thermal resistance, θ_{JC} (junction to case), of the LME49830TB is 4°C/W. Using Thermalloy Thermacote thermal compound, the thermal resistance, θ_{CS} (case to sink), is about 0.2°C/W. Since convection heat flow (power dissipation) is analogous to current flow, thermal resistance is analogous to electrical resistance, and temperature drops are analogous to voltage drops, the power dissipation out of the LME49830 is equal to the following:

$$P_{DMAX} = (T_{JMAX} - T_{AMB}) / \theta_{JA} \text{ (W)} \quad (1)$$

where

- $T_{JMAX} = 150°C$
- T_{AMB} is the system ambient temperature
- $\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$



Once the maximum package power dissipation has been calculated, the maximum thermal resistance, θ_{SA}, (heat sink to ambient) in °C/W for a heat sink can be calculated. This calculation is made using Equation (2) which is derived by solving for θ_{SA} in Equation (1).

$$\theta_{SA} = [(T_{JMAX} - T_{AMB}) - P_{DMAX}(\theta_{JC} + \theta_{CS})] / P_{DMAX} \text{ (°C/W)} \quad (2)$$

Again it must be noted that the value of θ_{SA} is dependent upon the system designer's amplifier requirements. If the ambient temperature that the audio amplifier is to be working under is higher, then the thermal resistance for the heat sink, given all other things are equal, will need to be smaller (better heat sink).

PROPER SELECTION OF EXTERNAL COMPONENTS

Proper selection of external components is required to meet the design targets of an application. The choice of external component values that will affect gain and low frequency response are discussed below.

The gain is set by resistors R_f and R_i for the non-inverting configuration shown in Figure 1. The gain is found by Equation 3 below:

$$A_V = 1 + R_f / R_i \text{ (V/V)} \quad (3)$$

For best noise performance, lower values of resistors are used. For the LME49830 the gain should be set no lower than 26dB. Gain settings below 26dB may experience instability.

The combination of R_i with C_i (see Figure 1) creates a high-pass filter. The low frequency response is determined by these two components. The -3dB point can be found from Equation 4 shown below:

$$f_i = 1 / (2\pi R_i C_i) \text{ (Hz)} \quad (4)$$

If an input coupling capacitor is used to block DC from the inputs as shown in Figure 1, there will be another high-pass filter created with the combination of C_{IN} and R_{IN}. When using a input coupling capacitor R_{IN} is needed to set the DC bias point on the amplifier's input terminal. The resulting -3dB frequency response due to the combination of C_{IN} and R_{IN} can be found from Equation 5 shown below:

$$f_{IN} = 1 / (2\pi R_{IN} C_{IN}) \text{ (Hz)} \quad (5)$$

With large values of R_{IN} oscillations may be observed on the outputs when the inputs are left floating. Decreasing the value of R_{IN} or not letting the inputs float will remove the oscillations. If the value of R_{IN} is decreased then the value of C_{IN} will need to increase in order to maintain the same -3dB frequency response.

AVOIDING THERMAL RUNAWAY WHEN USING BIPOLAR OUTPUT STAGES

When using a bipolar output stage with the LME49830, the designer must beware of thermal runaway. Thermal runaway is a result of the temperature dependence of V_{BE} (an inherent property of the transistor). As temperature increases, V_{BE} decreases. In practice, current flowing through a bipolar transistor heats up the transistor, which lowers the V_{BE}. This in turn increases the current again, and the cycle repeats. If the system is not designed properly, this positive feedback mechanism can destroy the bipolar transistors used in the output stage.

One of the recommended methods of preventing thermal runaway is to use a heat sink on the bipolar output transistors. This will keep the temperature of the transistors lower. A second recommended method is to use emitter degeneration resistors. As current increases, the voltage across the emitter degeneration resistor also increases, which decreases the voltage across the base and emitter. This mechanism helps to limit the current and counteracts thermal runaway.

A third recommended method is to use a "V_{BE} multiplier" to bias the bipolar output stage. The V_{BE} multiplier consists of a bipolar transistor and two resistors, one from the base to the collector and one from the base to the emitter. The voltage from the collector to the emitter (also the bias voltage of the output stage) is $V_{BIAS} = V_{BE}(1+R_{CB}/R_{BE})$, which is why this circuit is called the V_{BE} multiplier. When V_{BE} multiplier transistor (Q_{VBE} in Figure 1) is mounted to the same heat sink as the bipolar output transistors, its temperature will track that of the output transistors. The bias voltage will be reduced as the Q_{VBE} heats up reducing bias current in the output stage.

The bias circuit used in Figure 1 is a modified V_{BE} multiplier circuit. The additional resistor, R_{B1}, sets a temperature independent portion of the bias voltage while the rest of the V_{BE} multiplier circuit will adjust bias voltage with temperature. This reduces the amount of bias voltage change with heat sink temperature for steady bias current with the output devices shown.

BIAS SETTING

Setting the bias voltage and resulting output stage bias current is done by adjusting the R_{BIAS} resistor. If temperature compensation is not needed for the bias stage, the bias stage can consist of just a resistor and a sufficient capacitor. The output current from the two BIAS pins is typically 2mA and setting the output stage bias voltage is a simple Ohm's Law calculation. The bias voltage can be set up to 16V for maximum flexibility for use with a wide range of different MOSFET types. The wide range of bias voltage also allows for setting the output stage bias current for different performance levels.

OPTIMIZING EXTERNAL COMPONENTS

External component values, types and placement are highly design dependent. Values affect performance such as stability, THD+N, noise, slew rate and sonic performance. Optimizing the values can have a significant effect on total audio performance.

In a simple output stage design with one MOSFET device per side, as shown in Figure 1, the R_E resistors are often considered optional. The $R_{DS(on)}$ of the devices serve a similar purpose. As the output stage is scaled up in number of devices the value of R_E will need to be optimized for best performance. Typical values range from 0.1Ω to 0.5Ω.

The value of the gate resistors affect stability and slew rate. The capacitance of the output device should be considered when determining the value of the gate resistor. The values shown in Figure 1 represent a typical value or a starting value from which optimization can occur.

The compensation capacitor (C_C) is one of the most critical external components in value, placement and type. The capacitor should be placed close to the LME49830 and a silver mica type will give good performance. The value of the capacitor will affect slew rate and stability. The highest slew rate possible while also maintaining stability through out the power and frequency range of operation results in the best audio performance. The value shown in Figure 1 should be considered a starting value with optimization done on the bench and in listening testing.

The input capacitor (C_{IN}) is shown in Figure 1 for protection against sources that may have a DC bias. For best audio performance, the input capacitor should not be used. Without the input capacitor, any DC bias from the source will be transferred to the load.

The feedback capacitor (C_i) is used to set the gain at DC to unity. Because a large value is required for a low frequency -3dB point, the capacitor is an electrolytic type. An additional small value, high quality film capacitor may be used in parallel to improve high frequency sonic performance. If DC offset in the output stage is acceptable without the feedback capacitor, it may be removed but DC gain will now be equal to AC gain.

SUPPLY BYPASSING

The LME49830 has excellent power supply rejection and does not require a regulated supply. However, to eliminate possible oscillations all op amps and power op amps should have their supply leads bypassed with low inductance capacitors having short leads and located close to the package terminals. Inadequate power supply bypassing will manifest itself by a low frequency oscillation known as “motorboating” or by high frequency instabilities. These instabilities can be eliminated through multiple bypassing utilizing a large tantalum or electrolytic capacitor (10µF minimum) which is used to absorb low frequency variations and a small capacitor (0.1µF) to prevent any high frequency feedback through the power supply lines. These capacitors should be located as close as possible to the supply pins of the LME49830. An additional 0.1µF - 1µF capacitor connected between the V_{CC} to V_{EE} pins of the LME49830 is recommended and each output device should have adequate bypassing at each supply terminal.

OUTPUT SENSING

The Output Sense pin Osense must be connected to the system output as shown in Figure 1. This connection completes the return path to feedback the output voltage to the mute gain circuitry inside LME49830. If the Osense pin is not connected to the output or it is floated, high voltage generated from the output stage may cause damage to the speaker or load.

Demonstration Board Schematic

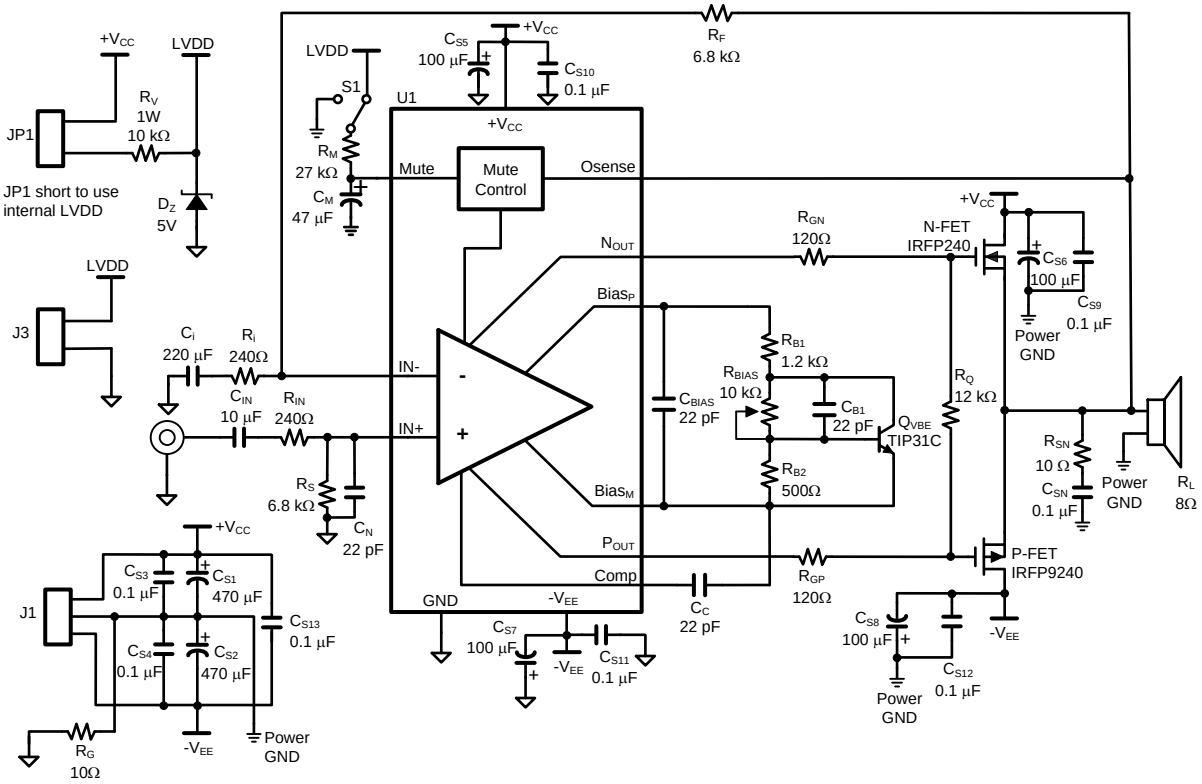


Figure 33. LME49830 Demo Board with Mute Function Schematic

Demonstration Board Layout

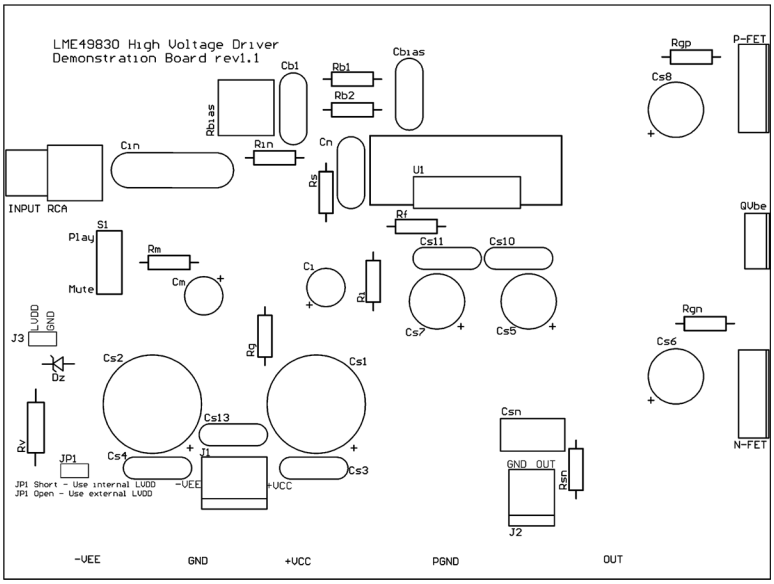


Figure 34. Top Silkscreen

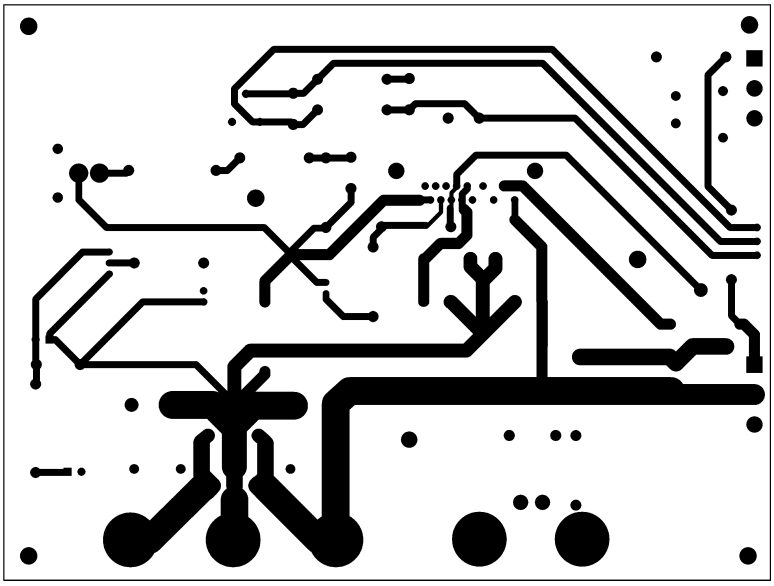


Figure 35. Top Layer

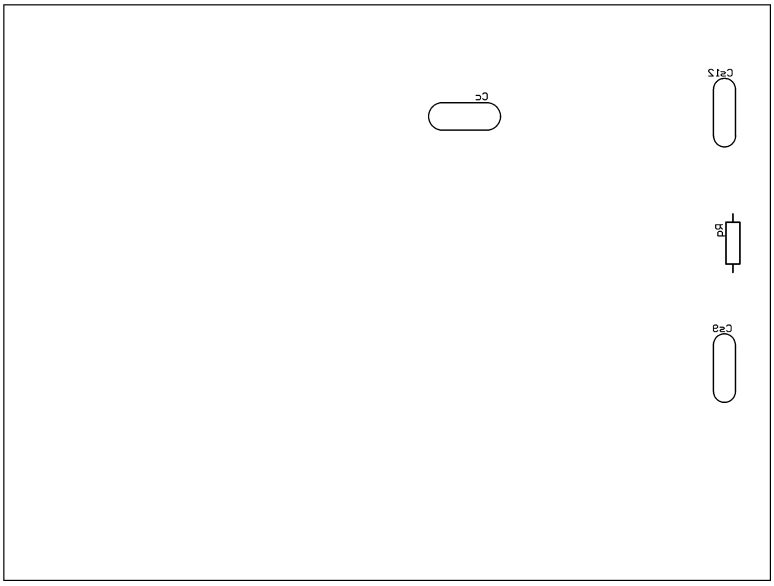


Figure 36. Bottom Silkscreen Layer

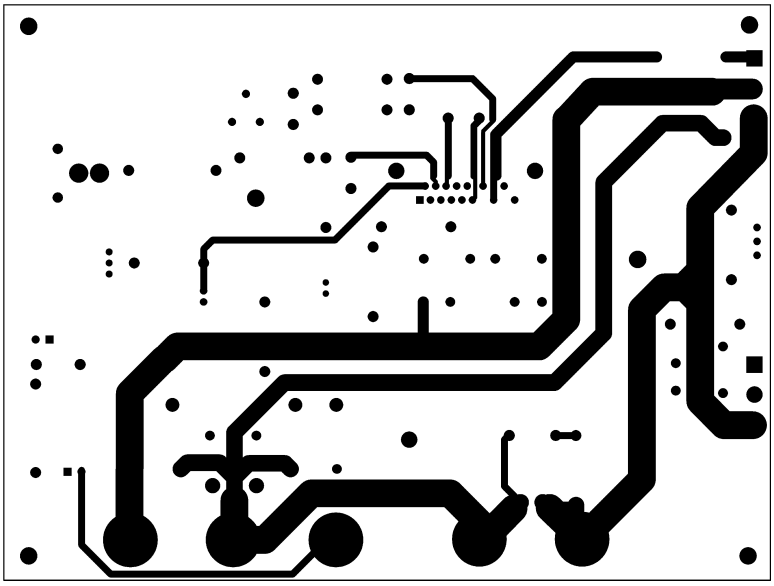


Figure 37. Bottom Layer

Demonstration Board Bill of Materials

Item	Description	Designator	Part Number	Quantity	Value	Supplier
1	High Perf MOSFET Power Amplifier Input Stage	U1	LME49830TB	1	200V, 60mA	Texas Instruments
2	Mica Capacitor	C_{BIAS}, C_C, C_N, C_{B1}	495–666	4	22pF	RS
3	Aluminum Electrolytic Capacitor	Ci	EEUFC1C221	1	220µF, 16V	Panasonic
4	Metal Polyester Film Cap	Cin	ECQE1106KF	1	10µF, 100V	Panasonic
5	Aluminum Electrolytic Capacitor	Cs1, Cs2	EEUFC2A471	2	470µF, 100V	Panasonic
6	Metal Polyester Film Cap	Cs3, Cs4, Cs9, Cs10, Cs11, Cs12, Cs13	ECQE2104KF	7	0.1µF, 200V	Panasonic
7	Zener Diode	Dz	TZX5V1C	1	5V	Vishay
8	RCA Jack	INPUT RCA	N/A	1	N/A	N/A
9	Header, 3-pin	J1	N/A	1	N/A	N/A
10	Header, 2-Pin	J2	N/A	1	N/A	N/A
11	Female Bannana Jack - Red	$+V_{CC}$	2142-2	1	N/A	Pomona Electronics
12	Female Bannana Jack - Red	$-V_{EE}$	2142-2	1	N/A	Pomona Electronics
13	Female Bannana Jack - Black	GND	2142-0	1	N/A	Pomona Electronics
14	Female Bannana Jack - Black	PGND	2142-0	1	N/A	Pomona Electronics
15	Female Bannana Jack - Red	OUT	2142-2	1	N/A	Pomona Electronics
16	Header, 2–Pin	JPI, J3	5-826646-0	2	N/A	Tyco Electronics
17	HEXFET Power N-MOSFET	N-FET	IRFP240	1	250V, 15A	International Rectifier
18	HEXFET Power P-MOSFET	P-FET	IRFP9240	1	–200V, –12A	International Rectifier
19	Resistor	R_{B1}	ERO-25PHF1201	1	1.2kΩ	Panasonic
20	Resistor	R_{B2}	ERO-25PHF5000	1	500Ω	Panasonic
21	Potentiometer	R_{BIAS}	63M-T607-103	1	10kΩ	Vishay
22	Resistor	R_F, R_S	ERO-25PHF6801	2	6.8kΩ	Panasonic
23	Resistor	R_{GN}, R_{GP}	ERG-12SJ121	2	120Ω, 0.5W	Panasonic

Item	Description	Designator	Part Number	Quantity	Value	Supplier
24	Resistor	R_i, R_{IN}	ERO-25PHF2400	2	240Ω	Panasonic
25	Resistor	R_M	ERO-25PHF2702	1	27kΩ	Panasonic
26	Resistor	R_V	ERG1SJ103	1	10kΩ, 1W	Panasonic
27	Resistor	R_Q	ERO-25PHF1202	1	12kΩ	Panasonic
28	Resistor	R_G	ERG-12SJ100	1	10Ω, 0.5W	Panasonic
29	Single-Pole, Double-Throw Switch	S1	SS40010F-0102-2.5G-NN	1	N/A	Alpha
30	Metal Polyester Film Cap	Csn	ECQE2104KF	1	0.1µF, 200V	Panasonic
31	Resistor	Rsn	ERO-25PHF10R0	1	10Ω,0.25W	Panasonic
32	Heat Sink for N-FET, P-FET, Q_{VBE}	N/A	150018	1	0.85°C/W	Farnell Newark
33	Heat Sink Clip for U1	N/A	403-207	1	N/A	RS
34	Sil-pad Insulator	N/A	169-2177	4	N/A	RS
35	Heat Sink for U1–LME49830	N/A	403178	1	10°C/W	RS
36	Aluminum Electrolytic Capacitor	Cs5, Cs6, Cs7, Cs8	EEUFC2A101	4	100µF, 100V	RS
37	Aluminum Electrolytic Capacitor	C_M	EEUFC1E470	1	47µF, 25V	Panasonic
38	Transistor	Q_{VBE}	TIP31C	1	100V	On Semiconductor

REVISION HISTORY

Rev	Date	Description
1.0	01/09/08	Initial release.
1.01	01/16/08	Deleted the Limit values on Vnoise (EC table)..
1.02	01/22/08	Changed limit values on Vnoise, I_B, and I_{AB}.
1.03	01/24/08	Updated the Typical demo ckt diagram and the App ckt diagram.
D	04/05/13	Changed layout of National Data Sheet to TI format.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LME49830TB/NOPB	OBSOLETE	TO-OTHER	NDN	15		TBD	Call TI	Call TI	-20 to 75	LME49830 TB	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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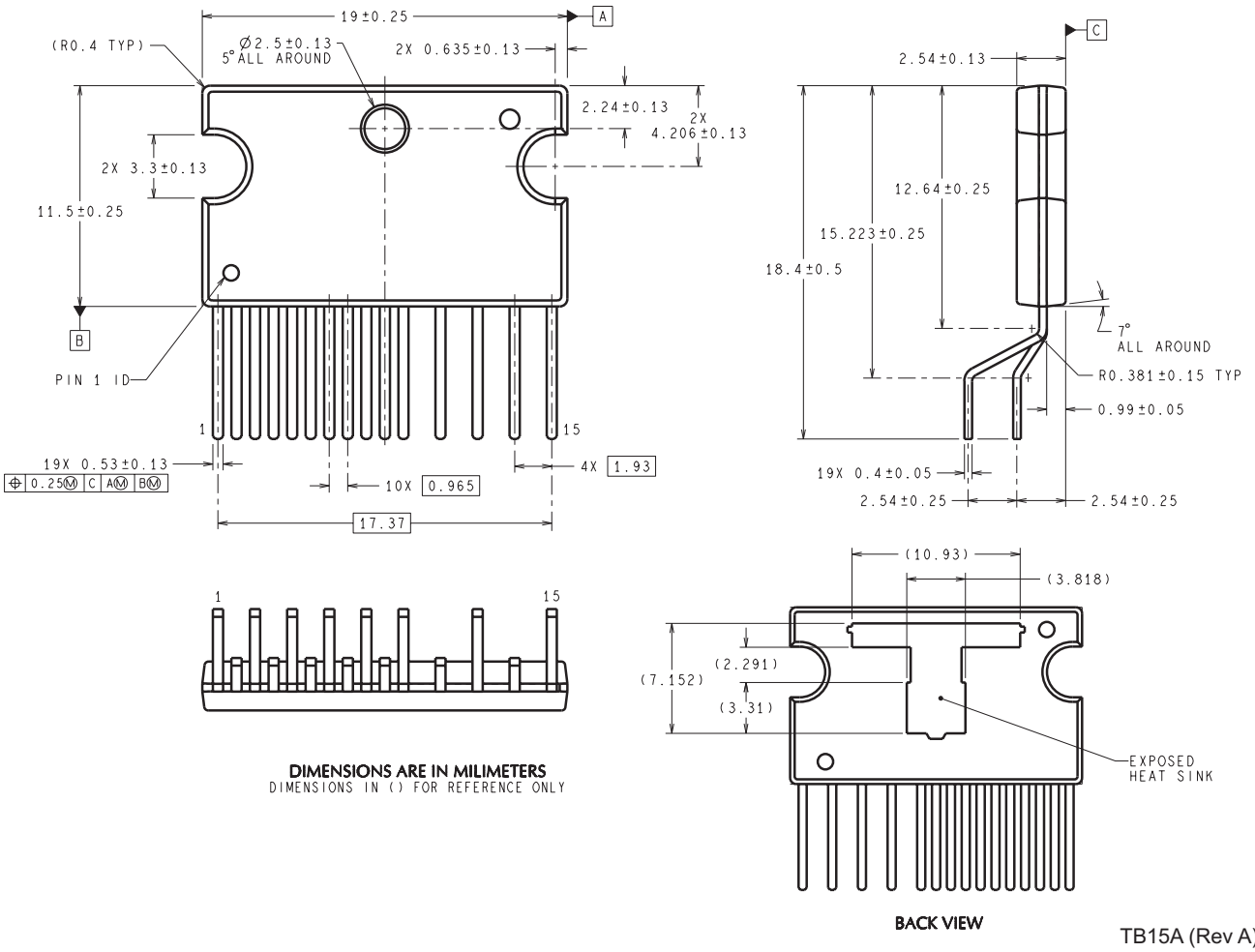

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